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Description

METHOD OF ACCESSING DATA OF A COMPUTER SYSTEM

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a computer system, and more particularly, to a method of accessing data of the computer system with a digital signal processing chip having a static random access memory (SRAM) and a cache memory.

[0003] 2. Description of the Prior Art

[0004] The dramatic development of communications technologies demands high-efficiency digital signal processing (DSP) chips. A DSP chip is capable of executing a plurality of operations in a single instruction cycle and can substitute for a central processing unit (CPU) to execute complex arithmetic operations, such as convolution and fast Fourier transform (FFT), so that the CPU can concentrate

on system control.

[0005] Please refer to Fig.1, which is a function block diagram of a computer system 10 according to the prior art. The computer system 10 comprises a DSP chip 12 and a dynamic random access memory (DRAM) 14 electrically connected to the DSP chip 12 via a plurality of address lines 16 and data lines 18. The DSP chip 12 is capable of accessing and processing data of the DRAM 14 through the address lines 16 and data lines 18. In general, time for the DSP chip 12 to access data of the DRAM 14 through the address lines 16 and data lines 18 is approximately six times longer than time needed to process these accessed data (clock cycle). For example, if the DSP chip 12 has a clock cycle ranging between 120 MHz to 250 MHz, time for the DSP chip 12 to access one set of data is around 48-24 nanoseconds, which is far longer than 4-8 nanoseconds, time for the DSP chip 12 to process these data. In conclusion, how fast the DSP chip 12 accesses data of the DRAM 14 dominates the efficiency of the DSP chip 12.

[0006] A concept of embedding an embedded memory is introduced to improve the efficiency of the DSP chip 12. Please refer to Fig.2, which is a function block diagram of an-

other computer system 20 according to the prior art. The computer system 20 comprises a DSP chip 22 and a DRAM 24 electrically connected to the DSP chip 22 via a plurality of address lines 26 and data lines 28. The DSP chip 22 comprises a static random access memory (SRAM) 30. Because time for the DSP chip 22 to access one set of data of the SRAM 30 is around only 3 nanoseconds, far shorter than 48-24 nanoseconds, data frequently used by the DSP chip 22 can be stored in the SRAM 30 in advance to improve the efficiency of the computer system 30.

[0007] However, the DSP chip 22 with the SRAM 30 embedded still has some shortcomings. For example, if a working space for the DSP chip 22 to store the frequent-used data is 12K words large, the SRAM 30 embedded into the DSP chip 22 also has to have a corresponding storing space of 12K words reserved. In general, a program code the DSP chip 22 manages has a size of 4K words for example, smaller than 12K words, so the SRAM 30 has two thirds of its storing space idled. This idle storing space of the SRAM 30 not only increase cost to produce the DSP chip 22, since the SRAM 30 occupies major area of the DSP chip 22, the idle storing space also increases the bulk of the DSP chip 22.

[0008] In addition, the SRAM 30 having a constant storing space (for example 12K words) limits the DSP chip 22 to execute an application program demanding a memory space less than 12K words.

[0009] Lastly, because a direct memory access (DMA) controller has to be introduced to manage data communications between the SRAM 30 of the DSP chip 22 and the DRAM 24, a control program code stored in the DSP chip 22 to control the DMA controller has to be changed accordingly if data allocation of the SRAM 30 has changed.

SUMMARY OF INVENTION

[0010] It is therefore a primary objective of the claimed invention to provide a method of accessing data of a computer with a DSP chip having an embedded cache memory and an SRAM.

[0011] According to the claimed invention, the method is proposed for accessing data of a computer system. The computer system has a first memory, a second memory, an address decoder, a digital signal processing unit electrically connected to the address decoder, a demultiplexer having an input end electrically connected to the digital signal processing unit, a first output end electrically connected to the second memory, and a control end electri-

cally connected to the address decoder, and a multiplexer having an output end electrically connected to the digital signal processing unit, a first input end electrically connected to the second memory, and a control end electrically connected to the address decoder. The method has following steps:(a)providing the digital signal processing unit with a cache memory electrically connected to the first memory, the cache memory having an input end electrically connected to a second output end of the demultiplexer, an output end electrically connected to a second input end of the multiplexer, and a tag stored with an address data; and (b)when the digital signal processing unit generates an address signal, (c) controlling the demultiplexer with the address decoder according to the address signal to transfer the address signal either to the cache memory or to the second memory and to enable the digital signal processing unit to receive contents via the multiplexer either from the cache memory or from the second memory, (d) comparing the address signal with the address data if the address signal is transmitted to the cache memory, and either transmitting contents of the cache memory corresponding to the address signal via the multiplexer to the digital signal processing unit if the ad-

dress signal matches the address data or updating contents of the cache memory corresponding to the address signal with contents of the first memory corresponding to the address signal, (e) updating the address data with the address signal and transmitting the updated contents of the cache memory via the multiplexer to the digital signal processing unit, and (f) transmitting contents of the second memory corresponding to the address signal via the multiplexer to the digital signal processing unit if the address signal is transmitted to the second memory.

[0012] The address decoder, the second memory, the digital signal processing unit, the demultiplexer, the multiplexer, and the cache memory are all integrated into a single digital signal processing chip.

[0013] In the preferred embodiment, the first memory is a DRAM and the second memory is an SRAM.

[0014] It is an advantage of the claimed invention that a digital signal processing chip has not only an SRAM but also a cache memory embedded and is capable of storing frequently-used data into the cache memory to improve the efficiency of a computer which the digital signal processing chip is installed in.

[0015] These and other objectives of the claimed invention will

no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0016] Fig.1 is a function block diagram of a computer system according to the prior art.

[0017] Fig.2 is a function block diagram of another computer system according to the prior art.

[0018] Fig.3 is a function block diagram of a computer system of a preferred embodiment according to the present invention.

[0019] Fig.4 is a flow chart of a method of accessing data of the computer shown in Fig.3 according to the present invention.

Detailed Description

[0020] Please refer to Fig.3, which is a function block diagram of a computer system 40 of the preferred embodiment according of the present invention. The computer system 40 comprises a DSP chip 42 and a DRAM 44 electrically connected to the DSP chip 42 via a plurality of address lines 46 and data lines 48. The DSP chip 42 comprises an SRAM

50, an address decoder 52, a digital signal process unit 54 electrically connected to the address decoder 52, a delmultiplexer 56, a multiplexer 58, and a cache memory 60 having a tag (not shown) for storing address information. The demultiplexer 56 comprises an input end I electrically connected to the digital signal processing unit 54, a first output end O_1 electrically connected to the SRAM 50, and a control end D_c electrically connected to the address decoder 52. The multiplexer 58 comprises an output end O electrically connected to the digital signal processing unit 54, a first input end I_1 electrically connected to the SRAM 50, and a control end D_c electrically connected to the address decoder 52. The cache memory 60 comprises an input end electrically connected to a second output end O_2 of the delmultiplexer 56, and an output end electrically connected to a second input end I_2 of the multiplexer 58.

[0021] Since time for the digital signal processing unit 54 to access one set of data of the cache memory 60 is only 4 nanoseconds, far shorter than 42 nanoseconds, time for the digital signal processing unit 54 to access one set of data of the DRAM 44, the DSP chip 40 can promote the efficiency of the computer system 40 by selectively storing

frequently-used data and program codes to the cache memory 60.

[0022] In the preferred embodiment of the present invention, the SRAM 50 has a memory space of 4K, and the cache memory 60 has a memory space of 4K as well. Of course, the SRAM 50 as well as the cache memory 60 can have memory space of a variety of sizes in accordance with practical demands.

[0023] Address lines 46 and data lines 48 installed in the DSP chip 42, for example address lines connecting the digital signal processing unit 54 and the demultiplexer 56 and data lines connecting the multiplexer 58 and the cache memory 60 or the SRAM 50, have a Harvard structure. Because time for address calculation is usually no less than that for data calculation in the DSP chip 42, the DSP chip 42 of the Harvard structure can further comprise an address generator (not shown) to accelerate the address calculation.

[0024] A method 100 for the DSP chip 42 of the computer system 40 to process data or to execute program codes is described as follows: Please refer to Fig.4, which is a flow chart of the method 100 of accessing data of the computer system 40 according to the present invention. The

method 100 comprises following steps:

[0025] Step 101:Start;

[0026] Step 102:Generate a control signal to control the demultiplexer 56 and the multiplexer 58 according to an address signal with the address decoder 52 when the digital signal processing unit 54 outputs the address signal;

[0027] Step 104:Determine whether or not the address signal corresponds to the SRAM 50, if yes, go to step 120, else, go to step 140;

[0028] Step 120:Control the demultiplexer 56 to transfer the address signal via the demultiplexer 56 to the SRAM 50 and control the multiplexer 58 to enable the digital signal processing unit 54 to receive data transferred from the SRAM 50 via the multiplexer 58;

[0029] Step 122:Transfer data of the SRAM 50 corresponding to the address signal via the multiplexer 58 to the digital signal processing unit 54, go to step 198;

[0030] Step 140:Control the demultiplexer 56 to transfer the address signal via the demultiplexer 56 to the cache memory 60 and control the multiplexer 58 to enable the digital signal processing unit 54 to receive data transferred from the cache memory 60 via the multiplexer 58;

[0031] Step 142:Compare the address signal with the address in-

formation stored in the tag of the cache memory 60;

[0032] Step 144:If the address signal hits the address information, then go to step 160, else (misses) go to step 180;

[0033] Step 160:Transfer data of the cache memory 60 corresponding to the address signal via the multiplexer 58 to the digital signal processing unit 54, go to step 198;

[0034] Step 180:Update data of the cache memory 60 corresponding to the address signal with data of the DRAM 44 corresponding to the address signal;

[0035] Step 182:Update the address information of the tag of the cache memory 60 with the address signal:

[0036] Step 184:Transfer the updated data of the cache memory 60 corresponding to the address signal via the multiplexer 58 to the digital signal processing unit 54; and

[0037] Step 198:Ends.

[0038] In step 180, the address signal the DSP chip 42 generates can be used to address to a plurality of memory spaces of the DRAM 44 depending on a setting between the DSP chip 42 and the cache memory. The address signal is a logical address corresponding to a physical address of the DRAM 44, the physical address equal to a sum of the logical address and a configurable base address stored in the cache memory 60. These are well known in the prior art,

and further description is hereby omitted.

[0039] In contrast to the prior art, the present invention can provide a computer system 40, in which a DSP chip 42 comprises not only an SRAM but also a cache memory. Therefore, as mentioned above, the computer system 40 has advantages of small bulk, low cost, high efficiency, and remarkable expandability. In addition, with slight adjustment of the base address, the DSP chip 42 can further access data stored in another memory space other than the DRAM 44 with the cache memory 60.

[0040] Following the detailed description of the present invention above, those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.